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06EC56

# Fifth Semester B.E. Degree Examination, December 2012
# Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

**Note:** ***Answer FIVE full questions, selecting at least TWO questions from each part.***



## PART – A

1 a. Explain with structure the step-by-step flow of n-well fabrication process. **(10 Marks)**

b. Explain the design equations of MOS devices and VI characteristics for n and p devices. **(10 Marks)**

2 a. What are the different MOS layers? Draw the $\lambda$ based design rules for a transistor. **(07 Marks)**

b. A NMOS transistor has a threshold voltage of 0.75V, the body effect co-efficient equal to 0.54 compute the threshold voltage for $V_{SB} = 5V$ and $2\phi_F = -0.6$ V. **(05 Marks)**

c. Draw the circuit and stick diagram of two input NAND gate using CMOS logic, use standard colour or monochrome codes. **(08 Marks)**

3 a. Explain the Pseudo-NMOS logic, structure and their salient features with example. **(08 Marks)**

b. Explain with the circuit the working principle of Bi-CMOS not gate and show the sub circuits of the output voltage. **(08 Marks)**

c. Implement the complementary CMOS logic, for the expression $Y = \overline{A \cdot (B+C) \cdot (D+E)}$. Show the design step clearly. **(04 Marks)**

4 a. With a neat circuit diagram and waveform, explain the principle of operation of a dynamic logic and what are the advantages and disadvantages. **(10 Marks)**

b. Explain with circuit diagram the super buffers with inverting type and non-inverting type of nmos. **(10 Marks)**

## PART – B

5 a. Discuss the architectural issues to be followed in the design of a VLSI subsystems. **(10 Marks)**

b. Design a 4:1 multiplexer using nmos logic and CMOS logic. **(10 Marks)**

6 a. Explain the important general consideration in CMOS design process. **(07 Marks)**

b. Explain the implementation of ALU functions with a standard adder. **(08 Marks)**

c. Define regularity in process illustration. **(05 Marks)**

7 a. Discuss the important factors of system timing consideration. **(10 Marks)**

b. Draw the circuit and stick diagram. Explain n-MOS pseudo-static memory cell. **(10 Marks)**

8 Write short notes on :

a. I/O Pads

b. Test and testability

c. LSSD

d. BIST **(20 Marks)**

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